UNIVERSITI PUTRA MALAYSIA

DEVELOPMENT OF TEST PROCEDURE FOR CMOS OPERATIONAL AMPLIFIER APPLICATION CIRCUITS

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By

IZHAL BIN ABDUL HALIN

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of the Requirement for the Degree of Master of Science

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DEDICATION

To my parents,

Father (Abdul Halin) and Mother (Sharifah Zaleha),

Brother (Alfian) and Sister (Afiza)

guardians,

Auntie (Che Puteh) and Cousin (Tunku Nurul Ashiken)

and my loving wife

(Farawahida)

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Master of Science

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IZHAL BIN ABDUL HALIN

January 2002

Chairman : Dr. Bambang Sunaryo Suparjo

Faculty : Engineering

The integrated circuit (IC) is an ultra-small and fragile electrical system. A chip is basically an IC placed in a protective black plastic casing. The only contact the outside world has with the IC is through the chips input-output and power supply pins. ICs are also prone to damage and to locate damages inside a chip requires special probing techniques. These techniques are incorporated from the beginning of the design stage of a chip. Design for Testability (DFT) is a method applied to the design stage of chips such that electrical testing of the chips at the end of the production stage is greatly simplified.

For a chip manufacturer, DFT helps cut production cost by shortening the time to test finished chips which eventually decreases the time to market the chip. Built-In Self Test (BIST) chips, an outcome of DFT, are ICs designed with extended circuitry dedicated to test its electrical behavior which eventually could inform a manufacturer where damage has occurred. The testing circuitry inside a BIST chip is complimented by a test pattern, which is a special signal that executes the actual testing. The main objective of this study is to develop a test procedure to test CMOS

Operational Amplifier (Op-Amp) application circuits. The focus in the development of the testing procedure is to find a suitable test pattern.

The study conducted results in the success of developing the said test procedure. The development of the test procedure is aided by a powerful computer software from Tanner Research Inc. called Tanner Tools. It is used for circuit simulation and development of a mask layout for an Op-Amp. The major findings of this thesis is that a faulty Op-Amp application circuit behaves differently from a faultless Op-Amp application circuit. From this finding a test pattern can be derived by comparing between faulty and faultless Op-Amp application circuit behavior through simulation. The only disadvantage of the test pattern is that it could only detect damages in the Op-Amp if the damages occurs only one at any given time. Thus it can be argued that in relation to DFT for an Op-Amp application circuit, it is not impossible for damages to be pin-pointed using the developed procedure.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Sarjana Sains

PEMBANGUNAN TATACARA PENGUJIAN UNTUK LITAR APLIKASI PENGUAT PENGENDALIAN CMOS

Oleh

IZHAL BIN ABDUL HALIN

Januari 2002

Pengerusi : Dr. Bambang Sunaryo Suparjo

Fakulti : Kejuruteraan

Litar bersepadu adalah sebuah sistem elektrik yang sangat kecil dan rapuh. Litar bersepadu yang diletakkan dalam sebuah bekas plastik hitam untuk tujuan perlindungan dikenali sebagai sebuah cip. Hubungan antara litar bersepadu dan dunia luar adalah hanya melalui pin-pin masukan-keluaran dan pin-pin kuasa cip tersebut. Litar besepadu juga boleh rosak dan teknik pengujian khas adalah perlu untuk mengenalpasti kerosakan tersebut. Teknik pengujian ini dilaksanakan dari permulaan pembikinan sesebuah cip iaitu pada peringkat rekabentuk. Rekabentuk Untuk Pengujian (DFT) adalah sebuah teknik yang diterapkan ke dalam proses merekabentuk sesebuah cip agar ujian elektrik yang dijalankan ke atas cip tersebut pada akhir proses pengeluaran dapat dipermudahkan.

DFT dapat membantu pengeluar cip mengurangkan kos produksi dengan memendekkan masa pengujian cip-cip yang siap, seraya itu mengurangkan masa untuk penjualan cip-cip tersebut. Cip-cip dengan kebolehan "Built-In Self Test" (BIST) adalah hasil penemuan teknik DFT dimana sesebuah cip BIST dibuat dengan litar tambahan yang dikhaskan untuk tujuan menguji tindakbalas elektrik cip

tersebut supaya pengeluar dapat mengesan lokasi sesebuah kerosakan dalam cip keluaran mereka. Litar pengujian dalam cip BIST disekalikan dengan sebuah corak pengujian iaitu suatu isyarat khas yang menjalankan kerja-kerja penguian. Tujuan utama kajian ini adalah untuk merekabentuk sebuah prosedur untuk menguji litar aplikasi penguat pengendalian CMOS. Untuk tujuan tersebuat, kajian ini mengkhusus untuk mencari sebuah corak pengujian yang sesuai bagi litar tersebut.

Pada akhir kajian ini, sebuah tatacara pengujian berjaya direkabentuk. Proses merekabentuk tatacara pengujian ini dibantu dengan penggunaan sebuah perisian komputer dari Tanner Inc. iaitu Tanner Tools. Ianya digunakan bagi tujuan simulasi litar dan untuk melukis gambarajah topeng bentangan sebuah litar penguat pengendalian. Penemuan utama kajian ini menunjukkan bahawa sebuah litar penguat pengendalian yang rosak bertindak luar biasa dari yang tidak rosak. Oleh itu dengan membuat perbandingan tindakbalas elektrik melalui simulasi komputer antara litar yang rosak dan tidak rosak, sebuah corak pengujian dapat direkabentuk. Kelemahan corak pengujian yang direkabentuk adalah ianya hanya dapat menunjukkan tempat kerosakan jika hanya satu kerosakan berlaku pada sesuatu masa. Namun begitu, boleh dikatakan bahawa merujuk kepada DFT untuk litar aplikasi penguat pengendalian, ianya tidak mustahil untuk mengesan kerosakan dengan menggunakan tatacara pengujian yang dihasilkan oleh kajian ini.

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Last but not least, a sincere thanks to my parents, brother and sister, wife, guardians, friends and loved ones, who have supported me with their undying love and wisdom. Without their existence, I surely would have no means to achieve what I have today.

I certify that an Examination Committee met on 21st January 2002 to conduct the final examination of Izhal bin Abdul Halin on his Master thesis entitled "Development of Test Procedure for CMOS Operational Amplifier Application Circuits" in accordance of Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulations 1981. The Committee recommends that the candidate be awarded the relevant degree. Members of the Examination Committee are as follows:

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DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations, which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

IZHAL BIN ABDUL HALIN

Date: 14 MARCH 2002

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1	Open Fault at Location 1
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5	Open Fault at Location 5
6	Open Fault at Location 6
A	Bridging Fault at Location A
A_v	Voltage Gain
B	Bridging Fault at Location B
BIST	Built-In-Self-Test
C	Bridging Fault at Location C
Cc	Feedback Capacitor
Cl^-	Chlorine Mobile Ion with Negative Charge
CMOS	Combinational Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
D	Bridging Fault at Location D
dB	Decibel
E	Bridging Fault at Location E
Gm	Transconductance
Hz	Hertz
I_a	Current at Branch A
I_{bias}	Biasing Current
IC	Integrated Circuit
I_d	Drain Current

I_{ddq}	Quiescent Power Supply Current
IEEE	Institute of Electrical and Electronic Engineers
I_f	Feedback Current
K^+	Kalium Mobile Ion with Positive Charge
L-Edit	Layout Editor
LVS	Layout vs. Schematic
MHz	Mega Hertz
MOS	Metal Oxide Semiconductor
ms	Millisecond
MSI	Medium Scale Integration
mV	Millivolt
Na^+	Natrium Mobile Ion with Positive Charge
NMOS	N-type MOS
Op Amp	Operational Amplifier
PCB	Printed Circuit Board
PMOS	P-type MOS
R	Resistance
R_b	Input Resistance b
R_{dd}	Vdd Current Sensing Resistor
R_f	Feedback Resistor
R_{id}	Op Amp Input Resistance
R_o	Op Amp Output Resistance
R_{out}	Output Resistor
R_s	Source Resistor
R_{ss}	Vss Current Sensing Resistor

S-Edit	Schematic Editor
SSI	Small Scale Integration
T-Spice	Tanner Spice
μF	Micro Farad
ULSI	Ultra Large Scale Integration
USA	United States of America
V	Volt, Node Voltage
V^-	Op Amp Inverting Input
V^+	Op Amp Non-Inverting Input
V_b	Input Voltage b
Vdd	Positive Power Supply
V_{GS}	Gate-Source Voltage
VLSI	Very Large Scale Integration
Vn	Op Amp Negative Input
V_{off}	Offset Voltage
Vp	Op Amp Positive Input
Vss	Negative Power Supply
V_{th}	Threshold Voltage
W-Edit	Wave Form Editor
Ω	Ohm
μs	Microsecond
(W/L)	Transistor Width to Length Ratio

CHAPTER 1

INTRODUCTION

The microchip, an ultra-small and fragile electrical system is prone to damage either during the fabrication process or during the operation of the device itself. In microchip production, the final products are all identical because a master mold is used for production. This also implies that there is a large possibility that defects of all the products are also the same in nature. If the cause and location of damage in a microchip is identified before mass production, it could be prevented.

Unlike in Digital Testing, Analog Testing is still new and needs to be developed. Although the testing methodology used in both digital and analog chips are almost alike, analog chips give more subjective test results. This is due to the nature of analog chips that have continuos flow of input-output signal levels. Digital chips on the other hand have only two input-output signal levels, which are logically true or false.

Thus in analog chip testing, the test parameters are continuos signal levels of the inputs and outputs. By careful analysis of these parameters, proper testing sequence could be devised in order to systematically test analog chips. At the end of this thesis, the reader would be guided through the steps taken to produce a flow of stages required to test a Two Stage CMOS Operational Amplifier (Op-Amp) which is a very popular device used in chips today.

1.1 Integrated Circuit and Testing

An Integrated Circuit (IC) is an ultra-small circuit that is built on a piece of semiconducting substrate. It is very fragile thus concealed inside a special plastic package for protection. Concealed in this special package it is commonly known as a chip. In a chip, the only contact the IC has with the outside world is through the chips power supply pins and interface pins (input-output pins).

The IC in a chip is also prone to damage, which occur either during the fabrication process of the IC or during operation of the chip. The damages or better known as faults will cause chips to behave abnormally. They alter chips transfer characteristics, which results in the unpredictability of output. Fortunately this fact could be used to identify where faults had occurred. To run these tests, special test equipment are used to generate test patterns and analyze tests results.

Modern day chip come with the ability to diagnose itself through a special system built into the chip. This special system could be activated whenever a chip has to be diagnosed. Once activated, the system will run tests designed especially for its host. Results from the test are obtained at the output pin(s) of the chip tested upon or known also as the Device Under Test (DUT). A chip with this special ability is known as Built-In-Self-Test (BIST) chips. The system dedicated for testing in a BIST chip is an extended circuitry designed into an IC. BIST chips could be tested without using expensive test equipment, but at what cost?